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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/088,028 | 03/14/2002 | Shinji Furusho | KUBOTA 0007 | 6569 |

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| EXAMINER | |
|---|---|
| COLEMAN, ERIC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/088,028 | FURUSHO, SHINJI | |
| | Examiner | Art Unit | |
| | Eric Coleman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling (patent No. 6,266,738) in view of Miller (patent No. 5,490,260) and Chang (patent No. RE37,305).

3. Dowling taught the invention substantially as claimed including a data processing (DP) system comprising:

CPU module (100) (e.g., see fig. 1);

Plurality of memory modules (e.g., see figs. 2, 11) each processor having a processor (150) and RAM core (140) (e.g., see fig. 1);

Plurality of sets of buses to make (a) connections between the CPU module and Memory modules or (b) connections among memory modules or that make (a) and (b) wherein the processors of the plurality of memory modules operate on an instruction given by the CPU module to the processors of the memory modules (e.g., see fig.11)(e.g., see col. 25, lines 53-col. 26, line 34); and

The architecture of a parallel computer manages at least one a series of data having stipulated relationship, (e.g., see fig. 5a and 5b)

4. Dowling did not expressly detail (claims 1,9) managing a table. Miller however taught a system with a CPU coupled to drams (e.g., see figs. 1, 2b). Miller taught compressed data partitions were provided in the DRAM memory with data stored in blocks of some fixed size. The partitions are capable of holding multiple blocks. The blocks may be compressed and the partitions are made of differing block sizes. This is taught as a virtual memory management system (e.g., see col. 2, line 45-col. 3, line 14). Miller taught tables indexed by page address (e.g. see col. 6, lines 28-67). Miller taught the mapping of the page being located in the secondary storage itself (e.g. see col. 7,lines 1-10) Miller taught use of the table in accessing data stored in memory (e.g. see col. 7, lines 1-19).. The Miller taught several types of memory being accessed. One type of memory being disk with a disk controller maintaining the table (e.g., see fig. 1). Accessing the other memory, the controller for the memory would search for the page address in a table maintained locally to determine if the page was stored in the partitions as compressed data and if so would read from the indicated location in the partitions (e.g., see col. 7, lines 1-19). As the teaching is understood where the table was located the memory partition the memory was DRAM where a DRAM controller was provided (e.g., see fig. 2b). The DRAM memory stores compressed data and the teaching of the memory storing address table locally both store compressed data.(e.g., see col. 8, lines 47-63). [this would correspond to maintaining the page table in the DRAM memory module that was used to access data in the memory module in the Dowling teachings].

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Dowling and Miller. Both references were directed toward the problems of use DRAM memory in a DP system. One of ordinary skill in the DP art would have been motivated to incorporate the Miller teachings of tables stored locally for accessing DRAM at least to provide a quicker access to data stored in the DRAM modules.

6. Miller did not specify the page table comprised a space ID. Chang, however taught managing a table with a segment Id (equivalent to space ID) (e.g., see fig. 3,4), virtual address with virtual page index and byte index (logical address a portion of a portion of the series of data) (e.g., see fig. 3), the size of the of the series of data (page size, e.g., see col. 20, lines 20-23 and fig. 12) . As to the access being in response to a instruction with logical address and Space ID since Chang taught segment ID and virtual address it would have been obvious to one of ordinary skill to use the segment ID and the logical address when the address was an immediate address within the instruction. The since the system of Dowling Miller and Chang would have been virtually addressed using segments and separate memory modules the address in the instruction would have had to indicate the module and the segment and that were the segment ID would have been required.

7. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Dowling and Chang. Both references were directed toward use of a partitioned memory in a DP system. One of ordinary skill in the DP art would have been motivated to incorporate the Chang teachings of the particulars of the addressing table

at least to provide for effective implementation of the virtual addressing of memory modules in Dowling.

8. As per the incorporation of the size of the portion of the series of data in the table Miller taught compressed and non-compressed versions of data stored in the memory. Therefore one of ordinary skill would have been motivated to store the size of the portion of the series of data (i.e., the compressed data stored in the page) at least to be able to quickly locate the beginning and end of a portion of data for accessing the data or storing an additional portion of data on the same page without wasting space.

9. Further the access of data (e.g., store or write operation) in the Dowling system would have included sending data to a bus and writing data to the DRAM as was well known in the art at the time of the claimed invention. Further Since Dowling taught processors within each memory module the processing of the accessed data would have been anticipated in the Dowling, Miller and Chang system. One of ordinary skill would have been motivated update the address table when data was stored at least to provide reliable access to data. [without updated address table the system would be vulnerable to inadvertently overwriting data already stored in the memory modules].

10. As per claim 2, Chang taught the processor has a controller that implements address translation (e.g., see col. 7, lines 32-57). Chang taught comparing segment ID and logical address to a corresponding tag and address for calculating physical address (e.g., see col. 11, lines 14-59 and col. 12, lines 10-22).

11. As per claim 3, Dowling taught sending to memory modules attribute signals for recognizing fetch cycles of CPU (the provides for synchronization of memory modules with CPU (e.g., see col. 5, lines 28-col. 6 line 19).

12. A per claim 4, Dowling taught switches for switching between buses and memory modules for controlling transfer between memory modules and between memory modules and CPU (e.g., see col. 18, lines 18-67).

13. As per claim 5,6 Dowling taught chained connections of buses (1140,1150,1160) between memory modules that provides multistage configuration (e.g. see fig. 11).

14. As to the limitations of claim 7, deletion of specific elements, insertion of elements into a series of data (i.e., page) or add a specific element to the end of a series of data (e.g., add data to the end of a page or the beginning of a next page) these are operations were well known in the art at the time of the claimed invention with respect to page addressed memories and therefore would have been anticipated with respect to the operation of the Dowling, Chang and Miller system. Since as discussed above table lookup was performed in the Miller and Chang teachings clearly one of ordinary skill would have been motivated to use the table for accessing the memory for well known operations such as storing, loading, deletion of data.

15. As per claim 8, Miller taught translating (converting a value) addresses from virtual to real for giving a specific modification to elements (the specific modification is modifying the length of the address and the location of the address from virtual address space to physical address space (e.g., see col. 14, lines 1-16).

16. As per claims 10,11, Miller taught CPU links to a bus that is linked to a legacy memory connected to the bus (disk memory (e.g., see fig. 1). The connection of input devices such as keyboards computer mice, microphones etc was well known in the art and would have been used by one of ordinary skill in the art to facilitate the user to use the system of Miller, Dowling and Chang.

17. As per claims 12, 13 Dowling taught the buses connected in parallel between the memory modules (e.g., see fig. 11).

***Response to Arguments***

18. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER